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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/796,405	03/08/2004	Budong You	09464-029001	9025

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EXAMINER	
TON, MY TRANG	

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 12/14/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/796,405	YOU ET AL.	
	Examiner	Art Unit	
	My-Trang N. Ton	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-39 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-39 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 08 March 2004 is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Double Patenting

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington,* 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

1. Claims 1-8, 11-18 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-16 of U.S. Patent No. 6,529,056. Although the conflicting claims are not identical, they are not patentably distinct from each other because:

the present applications claim 1 reads on claim 1 of the prior patent (a first, main and second, helper FETs of the prior application reads on the first and second FETs);

the present applications claim 2 reads on claim 2 of the prior patent;

the present applications claim 3 reads on claim 3 of the prior patent;

the present applications claim 4 reads on claim 4 of the prior patent;

the present applications claim 5 reads on claim 5 of the prior patent;

the present applications claim 6 reads on claim 6 of the prior patent;

the present applications claim 7 reads on claim 7 of the prior patent;

the present applications claim 8 reads on claim 8 of the prior patent;

the present applications claim 11 reads on claim 9 of the prior patent;

the present applications claim 12 reads on claim 10 of the prior patent;

the present applications claim 13 reads on claim 11 of the prior patent;

the present applications claim 14 reads on claim 12 of the prior patent;

the present applications claim 15 reads on claim 13 of the prior patent;

the present applications claim 16 reads on claim 14 of the prior patent;

the present applications claim 17 reads on claim 15 of the prior patent;

the present applications claim 18 reads on claim 16 of the prior patent.

2. Claims 9-10, 19-22 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-16 of U.S. Patent No. 6,529,056 in view of Gergintschew, Patent No. 6,7,47,505 or Khemka et al, Patent No. 6,703,895.

As stated above, every element of the claimed invention recited in above claims can be seen in the prior patent. However, the prior art patent does not specifically disclosed "the first FET is an n-type CMOS FET" (claim 9) or "the first FET is an LDMOS transistor" (claim 10).

However, field effect transistors are well-known switching devices, these specific limitation drawn to the different type of FET, are seen as design expedients dependent upon the environment in which the circuit is deployed and the desired results. For

example, Gergintschew teaches the first FET (2) is an n-type CMOS FET or Khemka teaches the first FET (241) is an LDMOS transistor.

Therefore, it would have been obvious at the time of the invention was made for one skilled in the art to utilize these particular types of transistors (n-type CMOS FET or LDMOS transistor) because of the well-known advantages in performance and integration.

Regarding claims 19-22: FETs 2 and 3 (of Gergintschew) or FETs 241, 231, 221, 210 (of Khemka) are capable of performing limitations as recited in these claims.

3. Claims 23-36 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-14 of U.S. Patent No. 6,703,888. Although the conflicting claims are not identical, they are not patentably distinct from each other because:

the present applications claim 23 reads on claim 1 of the prior patent (a helper and main FETs of the prior application reads on the first and second FETs);

the present applications claim 24 reads on claim 2 of the prior patent;

the present applications claim 25 reads on claim 3 of the prior patent;

the present applications claim 26 reads on claim 4 of the prior patent;

the present applications claim 27 reads on claim 5 of the prior patent;

the present applications claim 28 reads on claim 6 of the prior patent;

the present applications claim 29 reads on claim 7 of the prior patent;

the present applications claim 30 reads on claim 8 of the prior patent;

the present applications claim 31 reads on claim 9 of the prior patent;

the present applications claim 32 reads on claim 10 of the prior patent;

the present applications claim 33 reads on claim 11 of the prior patent;

the present applications claim 34 reads on claim 12 of the prior patent;

the present applications claim 35 reads on claim 13 of the prior patent;

the present applications claim 36 reads on claim 14 of the prior patent.

4. Claims 37-39 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-14 of U.S. Patent No. 6,703,888 in view of Gergintschew, Patent No. 6,7,47,505 or Khemka et al, Patent No. 6,703,895.

The same motivation applied in paragraph (2) is applied to claims 37-39.

5. Claims 1-8, 11-18, 23-36 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-24 of U.S. Patent No. 6,433,614. Although the conflicting claims are not identical, they are not patentably distinct from each other because:

the prior patent claims: a circuit including a first field effect transistor, a second FET, a control circuit, a current sensing circuit, the second FET having a gate length (Lg) greater than the Lg of the first FET and an Ld greater than the Ld of the first FET, control circuit is coupled to the drain terminal, the control circuit is configured to impose a fixed delay, the first (or second) FET is designed for electrical performance superior to

that of the second (or first) FET, the first and second FETs and the control circuit are implemented as a single monolithic device, a current sensing circuit ;

wherein the instant application is now also claiming a power switch which includes all of the elements of the prior claims (for example: a first field effect transistor, a second FET, a control circuit, the second FET having a gate length Lg that is greater than an Lg of the first FET and having a length of a drain Ld that is greater than an Ld of the first FET, control circuit is coupled to the drain terminal, the control circuit is configured to impose a fixed delay, the first (or second) FET is designed for electrical performance superior to that of the second (or first) FET, the first and second FETs and the control circuit are implemented as a single monolithic device, and a current sensing circuit).

6. Claims 9-10, 19-22, 37-39 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-24 of U.S. Patent No. 6,433,614 in view of Gergintschew, Patent No. 6,7,47,505 or Khemka et al, Patent No. 6,703,895.

The same motivation applied to paragraph (2) is applied to claims 9-10, 19-22, 37-39.

Claim Rejections - 35 USC § 102

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the

applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-2, 6, 8-13, 18-22, 23-24, 27, 30-35, 37-39 are rejected under 35 U.S.C. 102(e) as being anticipated by Gergintschew (U.S Patent No. 6,747,505).

Gergintschew discloses in Figs. 1-3 a circuit including:

a first field effect transistor (2);

a second field effect transistor (3), the second FET having a gate length that is greater than or less than an Lg of the first FET and having a length of a drain that is greater than or less than Ld of the first FET (FET 3 has a smaller W/L ratio than FET 2, see col. 2, lines 59-2 and col. 4, lines 14-17);

and a control circuit (6) coupled to the gate terminal, the first gate and the second gate (2c, 3c) as recited in claim 1.

The control circuit (6) is configured to turn on the second FET (3) before turning on the first FET (2) (FET 3 turns on at time t1, and FET 2 turn on at time t2, see col. 4, lines 29-56) as recited in claim 2.

The control circuit (6) is configured to turn off the second FET (3) after turning off the first FET (2) (FET 2 is off at time t5, FET 3 is continues to deliver a large current until reaching its threshold voltage at time t6) as recited in claim 6.

The first FET (2) is capable of designed for electrical performance superior to that of the second FET (3) as recited in claim 8.

The first FET is an n-type CMOS FET (2) as recited in claim 9.

The first FET (2) is capable as LDMOS transistor as recited in claim 10.

The second FET (3) is capable designed for reliability performance superior to that of the first FET (2) as recited in claim 11.

Regarding claims 12-13: the limitation "single monolithic device" is inherent seen in col. 2, lines 63 – col. 3, line 17).

The second FET has an Lg smaller than an Lg of the first FET and Ld smaller than an Ld of the first FET (FET 3 has a smaller W/L ratio than FET 2, see col. 2, lines 59-2 and col. 4, lines 14-17) as recited in claim 18.

Regarding claims 19-22, FETs 2 and 3 are capable of performing limitations as recited in these claims.

The method claims 23-24, 27, 30-35, 37-39 are similarly rejected as the apparatus claims 1-2, 6, 8-13, 18-22.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to My-Trang N. Ton whose telephone number is 571-272-1754. The examiner can normally be reached on 7:00 a.m - 5:30 p.m.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on 571-272-1740. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

December 10, 2004

MY-TRANG NU TON
PRIMARY EXAMINER